B1 cont'd

The active elements in the second connection configuration have the identical or similar structure to the active element in the first connection configuration, and are connected to power lines of an internal circuit associated therewith but not connected to signal wires and so on in the internal circuit.

IN THE SPECIFICATION:

Please amend the specification as follows:

On page 6, line 13 please substitute the following paragraph:

B2

Further, as can be seen in Fig. 10B, for communicating signals between the internal circuits 4A, 4B, inter-circuit signal wires 12 for interconnecting the output element 12A of the internal circuit 4A and the input element 12B of the internal circuit 4B, and inter-circuit signal wires 13 for interconnecting the output element 13B of the internal circuit 4B and the input element 13A of the internal circuit 4A are also routed between the internal circuits 4A, 4B as many number of lines as required for communicating signals.

On page 6, line 21 please substitute the following paragraph:

B3

The output element 12A may comprise a single or a plurality of active elements such as transistors. For example, if the output element 12A is a CMOS invertor (see Fig. 11A), the output element 12A includes a p-type MOS (hereinafter called the "pMOS") transistor 12AP having a source connected to the power line 8A, a drain connected to the inter-circuit signal wire 12, and a gate connected to an internal signal wire SA within the internal circuit 4A; and an n-type MOS (hereinafter called the "nMOS") transistor 12AN having a source connected to the power line 9A, a drain connected to the inter-circuit signal wire 12, and a gate connected to the internal signal wire SA within the internal circuit 4A. The input element 12B also includes a pair

B3 cont'd

of transistors, pMOS transistor 12BP and nMOS transistor 12BN, having their sources connected to the power lines 8B, 9B, respectively, which have their gates connected to the inter-circuit signal wire 12, and their drains connected to an internal signal wire SB within the internal circuit 4B.

On page 7, line 11 please substitute the following paragraph:

B4

The input element 13A and the output element 13B, though signals are communicated in directions opposite to each other, each includes a similar transistor pair consisting of one pMOS transistor (13AP, 13BP) and one nMOS transistor (13AN, 13BN), with their drains or gates connected to the inter-circuit signal wire 13.

On page 9, line 11, please substitute the following paragraph:

B5

Specifically, as can be seen in Fig. 11D, basic cells of interest are formed with contact holes (see a black line in Fig. 11D) such as via holes at the centers thereof to connect the sources of the active elements 12AP, 12AN, 12BP, 12BN in the first connection configuration to the power lines 8A, 9A, 8B, 9B, respectively. In the internal circuit 4A, the internal signal wire SA is connected to the gate of the active element 12AP in the first connection configuration as well as to the gates of both the active elements 12AP, 12AN in the first connection configuration. Also, one end of the inter-circuit signal wire 12 is branched and connected to the drains of the active elements 12AP, 12AN in the first configuration at corners of the basic cells.

On page 12, line 6, please substitute the following paragraph:

B6

Also, in such a situation, if surge noise is introduced, for example, into the input/output terminal 7B (see Fig. 12C), the existence of the input protection circuit 3B for protecting the internal element 11B may adversely affect the other internal element 12B and so on. The surge